We claim:

1. A method for manufacturing a via in a metal interconnect structure comprising:

(a) providing a semiconductor substrate having a first metal layer formed thereon and an anti-reflective coating (ARC) on said first metal layer;

(b) forming a dielectric layer on said first metal layer;

(c) coating and patterning a photoresist layer on said dielectric layer to form a via opening in a via pattern in said photoresist layer;

(d) performing a first etch step to transfer the via through the dielectric layer; and

(e) performing a second etch step to transfer the via through the ARC layer and into said first metal layer, said via having a vertical sidewall and a via bottom with a curvature.

2. The method of claim **1** further comprised of stripping said photoresist layer, depositing a conformal diffusion barrier layer on the sidewall and via bottom, depositing a second metal layer to fill the via, and planarizing said second metal layer to be coplanar with said dielectric layer.

3. The method of claim **1** wherein said first metal layer is an Al/Cu alloy, AlSiCu or copper.

4. The method of claim **1** wherein said ARC layer is TiN, TaN, Ti/TiN, or Ta/TaN having a thickness from about 200 to 800 Angstroms.

5. The method of claim **1** wherein said dielectric layer has a thickness between about 2000 and 10000 Angstroms and is selected from a group including SiO_2, fluorine doped SiO_2, carbon doped SiO_2, poly(arylethers), polysilsesquioxanes, fluorinated polyimides, and benzocyclobutene.

6. The method of claim **1** wherein said via is part of a via pattern that includes isolated via holes, dense via holes, and semi-isolated via holes.

7. The method of claim **1** wherein said first etch step is performed with a plasma generated from a gas mixture comprised of a fluorocarbon, O_2, and an inert gas.

8. The method of claim **1** wherein said via bottom has an essentially continuous curvature that is defined by the lower portion of a circle having a radius R that connects points at the bottom of said vertical sidewall on opposite sides of the via and wherein R has a maximum value of 1.5 D and a minimum value of about 0.5 D where D is the diameter of said via.

9. The method of claim **8** wherein said second etch step is performed with a C_4F_8 flow rate of about 10 to 12 standard cubic centimeters per minute (sccm), an O_2 flow rate of about 3 to 5 sccm, a chamber pressure from about 40 to 50 mTorr, a chamber temperature between about 20°C and 60°C, and a RF power of about 1200 to 1500 Watts for a period of about 45 to 200 seconds.

10. The method of claim **1** wherein said via bottom is comprised of a flat bottom portion and a curved bottom corner and wherein the curvature of said curved bottom corner is defined by the portion of a circle having a radius R2 that connects a point on the bottom of said sidewall with the closest point at the edge of said flat bottom portion, said radius R2 having a minimum value of 0.25 D and a maximum value of about 0.5 D where D is the diameter of said via.

11. The method of claim **10** wherein said flat bottom portion has a circular shape from a top-down view, said circular shape having a diameter D3 where D3 + 2 R2 is equal to D.

12. The method of claim **10** wherein said second etch step is performed with a SF_6 flow rate of about 50 to 60 sccm, an inert gas flow, a chamber pressure from about 60 to 70 mTorr, a chamber temperature between about 20°C and 60°C, and a RF power of about 300 to 500 Watts for a period of about 12 to 60 seconds.

13. The method of claim **2** wherein said diffusion barrier layer is comprised of one or more of Ti, TiN, TiW, Ta, TaN, TaSiN, W, and WN.

14. The method of claim **2** wherein said diffusion barrier layer is a composite layer comprised of a first layer of Ti having a thickness from about 0 to 200 Angstroms and a second layer of TiN with a thickness of about 50 to 300 Angstroms.

15. The method of claim **2** wherein said second metal layer is an Al/Cu alloy, Al, W, or copper and is planarized by a chemical mechanical polish (CMP) step.

16. The method of claim **2** wherein the stripper that removes said photoresist is an organic solution that includes a corrosion inhibitor.

17. The method of claim **2** wherein said via is used to form an interconnect in a device that has an electromigration resistance which is higher than for a device having a via with an essentially flat bottom and which has sidewalls formed in said dielectric and ARC layers that extend into said first metal layer.

18. A method for manufacturing a via in an interconnect structure, comprising:

(a) providing a semiconductor substrate having a first metal layer formed thereon and an anti-reflective coating (ARC) on said first metal layer;

(b) forming a dielectric layer on said first metal layer;

(c) coating and patterning a photoresist layer on said dielectric layer to form a via opening in a via pattern in said photoresist layer; and

(d) performing an etch step to transfer the via through the dielectric layer, said etch stops on said ARC layer and forms a via with a sidewall and a flat bottom.

19. The method of claim **18** further comprised of stripping said photoresist layer, depositing a conformal diffusion barrier layer on the sidewall and via bottom, depositing a second metal layer to fill the via, and planarizing said second metal layer to be coplanar with said dielectric layer.

20. The method of claim **18** wherein said first metal layer is an Al/Cu alloy, AlSiCu, or copper.

21. The method of claim **18** wherein said ARC layer is TiN, TaN, Ti/TiN, or Ta/TaN having a thickness from about 200 to 800 Angstroms.

22. The method of claim **18** wherein said dielectric layer has a thickness between about 2000 and 10000 Angstroms and is selected from a group including SiO_2, fluorine doped SiO_2, carbon doped SiO_2, poly(arylethers), polysilsesquioxanes, fluorinated polyimides, and benzocyclobutene.

23. The method of claim **18** wherein said via is part of a pattern that includes isolated via holes, dense via holes, and semi-isolated via holes.

24. The method of claim **18** wherein said etch is performed with a gas mixture comprising a fluorocarbon, O_2, and an inert gas and with a higher chamber pressure and a lower Rf power than typically used for a similar etch through said dielectric layer that is followed by a second etch step into said ARC.

25. The method of claim **19** wherein said diffusion barrier layer is selected from one or more of Ti, TiN, TiW, Ta, TaN, TaSiN, W, and WN.

26. The method of claim **19** wherein said diffusion barrier layer is a composite layer comprised of a first layer of Ti having a thickness from about 0 to 200 Angstroms and a second layer of TiN with a thickness of about 50 to 300 Angstroms.

27. The method of claim **19** wherein said second metal layer is an Al/Cu alloy, Al, W, or copper and is planarized by a chemical mechanical polish (CMP) process.

28. The method of claim **19** wherein the stripper that removes said photoresist is an organic solution that includes a corrosion inhibitor.

29. The method of claim **19** wherein said via is used to form an interconnect in a device that has an electromigration resistance which is higher than a device with a via having a flat bottom and sidewalls formed in said dielectric and ARC layers that extend into said first metal layer.

30. The method of claim **18** further comprised of a second etch step immediately following said etch step through the dielectric layer, said second etch step stops in said ARC layer and forms a via having a flat bottom.

31. The method of claim **30** wherein the second etch step is performed with a C_4F_8 flow rate of about 10 to 12 standard cubic centimeters per minute (sccm), an O_2 flow rate of about 3 to 5 sccm, a chamber pressure from about 40 to 50 mTorr, a chamber temperature between about 20°C and 60°C, and a RF power of about 1200 to 1500 Watts for a period of about 50 to 80 seconds

32. A semiconductor device, comprising:

(a) a first metal layer formed on a semiconductor substrate;

(b) an anti-reflective (ARC) layer formed on said first metal layer;

(c) a dielectric layer formed on said ARC layer;

(d) a via hole comprised of a vertical sidewall and a via bottom having a curvature wherein said vertical sidewall is formed in said dielectric layer and extends through said ARC layer into said first metal layer and wherein said via bottom is formed in said first metal layer;

(e) a conformal diffusion barrier layer formed on the sidewall and bottom of said via hole and having a top surface that is coplanar with the dielectric layer; and

(f) a second metal layer formed on said diffusion barrier layer that fills said via hole and is coplanar with said dielectric layer and said diffusion barrier layer.

33. The semiconductor device of claim **32** wherein said first metal layer is comprised of an Al/Cu alloy, AlSiCu, or copper and has a thickness from about 1000 to 10000 Angstroms.

34. The semiconductor device of claim **32** wherein said ARC layer is TiN, TaN, Ti/TiN, or Ta/TaN having a thickness from about 200 to 800 Angstroms.

35. The semiconductor device of claim **32** wherein said dielectric layer has a thickness between about 2000 and 10000 Angstroms and is selected from a group including SiO_2, fluorine doped SiO_2, carbon doped SiO_2, poly(arylethers), polysilsesquioxanes, fluorinated polyimides, and benzocyclobutene.

36. The semiconductor device of claim **32** wherein said via is part of a via pattern that includes isolated via holes, dense via holes, and semi-isolated via holes.

37. The semiconductor device of claim **32** wherein said curvature in the via bottom is defined by the lower portion of a circle having a radius R that connects points at the bottom of said sidewall on opposite sides of the via and wherein R has a maximum value of 1.5 D and a minimum value of about 0.5 D where D is the diameter of said via.

38. The semiconductor device of claim **32** wherein said via bottom is comprised of a flat bottom portion and a curved bottom corner and wherein said curvature is defined by the portion of a circle having a radius R2 that connects a point on the bottom of said sidewall with the closest point at the edge of said flat bottom portion, said radius R2 having a minimum value of 0.25 D and a maximum value of about 0.5 D where D is the diameter of said via.

39. The semiconductor device of claim **38** wherein said flat bottom portion has a circular shape from a top-down view with a diameter D3 where D3 + 2 R2 is equal to D.

40. The semiconductor device of claim **32** wherein said diffusion barrier layer is comprised of one or more of Ti, TiN, TiW, Ta, TaN, TaSiN, W, and WN.

41. The semiconductor device of claim **32** wherein said diffusion barrier layer is a composite layer comprised of a first layer of Ti having a thickness from about 0 to 200 Angstroms and a second layer of TiN with a thickness of about 50 to 300 Angstroms.

42. The semiconductor device of claim **32** wherein said second metal layer is an Al/Cu alloy, Al, W, or copper.

43. The semiconductor device of claim **32** wherein said device has an electromigration resistance which is higher than a device comprised of a via with a flat bottom with no curvature and vertical sidewalls formed in said dielectric and ARC layers that extend into said first metal layer.

44. A semiconductor device, comprising:

(a) a first metal layer formed on a semiconductor substrate;

(b) an anti-reflective (ARC) layer formed on said first metal layer;

(c) a dielectric layer formed on said ARC layer;

(d) a via hole comprised of a vertical sidewall and a flat via bottom wherein said vertical sidewall is formed in said dielectric layer and stops on said ARC layer;

(e) a conformal diffusion barrier layer formed on the sidewall and bottom of said via hole, said diffusion barrier layer having a top surface that is coplanar with the dielectric layer; and

(f) a second metal layer formed on said diffusion barrier layer that fills said via hole and is coplanar with said dielectric layer and said diffusion barrier layer.

45. The semiconductor device of claim **44** further comprised of extending said via sidewall into said ARC where said flat bottom is formed.

46. The semiconductor device of claim **44** wherein said first metal layer is comprised of an Al/Cu alloy, AlSiCu, or copper and has a thickness from about 1000 to 10000 Angstroms.

47. The semiconductor device of claim **44** wherein said ARC layer is TiN, TaN, Ti/TiN, or Ta/TaN having a thickness from about 200 to 800 Angstroms.

48. The semiconductor device of claim **45** wherein said dielectric layer has a thickness between about 2000 and 10000 Angstroms and is selected from a group including SiO_2, fluorine doped SiO_2, carbon doped SiO_2, poly(arylethers), polysilsesquioxanes, fluorinated polyimides, and benzocyclobutene.

49. The semiconductor device of claim **44** wherein said via is part of a via pattern that includes isolated via holes, dense via holes, and semi-isolated via holes.

50. The semiconductor device of claim **49** wherein an isolated via in one part of said pattern has a flat bottom formed on said ARC layer and a via in a dense array in another part of said pattern has a flat bottom formed in said ARC layer.

51. The semiconductor device of claim **44** wherein said diffusion barrier layer is comprised of one or more of Ti, TiN, TiW, Ta, TaN, TaSiN, W, and WN.

52. The semiconductor device of claim **44** wherein said diffusion barrier layer is a composite layer comprised of a first layer of Ti having a thickness from about 0 to 200 Angstroms and a second layer of TiN with a thickness of about 50 to 300 Angstroms.

53. The semiconductor device of claim **44** wherein said second metal layer is an Al/Cu alloy, Al, W, or copper.

54. The semiconductor device of claim **45** wherein said device has an electromigration resistance which is higher than a device comprised of a via with a flat bottom formed in said first metal layer and with a vertical sidewall in said dielectric layer that extends through said ARC layer and into said first metal layer.